



Patent Application
Attorney Docket No.: 57941.000062
Client Reference No.: RA001.2003.1.C.US

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: :
:
Michael FARMWALD et al. :
: Group Art Unit: Unassigned
Appln. No.: 10/716,595 :
: Examiner: Unassigned
Filed: November 20, 2003 :
:
For: INTEGRATED CIRCUIT I/O USING :
A HIGH PERFORMANCE BUS :
INTERFACE :

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT

Sir:

In accordance with the duty under 37 C.F.R. § 1.56 of each individual associated with the filing and prosecution of the above-identified patent application (hereinafter, "associated individuals") to disclose all information known to that individual to be material to patentability, Applicant(s) hereby submits attached Form PTO-1449 (modified) listing cited references. This submission is made in accordance with 37 C.F.R. §§ 1.97 and 1.98 and § 609 of the Manual of Patent Examining Procedure.

The cited references, while believed to be of some relevance, are not necessarily considered to teach or suggest any aspect of the invention described and claimed in the above-

identified patent application. Applicant(s) hereby expressly reserves the right to swear behind the effective dates of any of the cited references. Applicant(s) further reserves the right to question the relevance, materiality, and/or prior art status of any of the cited references in whole, in part, or in combination, subsequent to the filing of this information disclosure statement. This information disclosure statement is also not to be construed as a representation that a search has, or has not, been conducted or that no better art exists. Rather, this information disclosure statement discloses only the best references of which the associated individuals are aware.


The Examiner is respectfully requested to consider each of the cited references, to indicate such consideration by initialing in the space provided next to each cited reference on the enclosed Form PTO-1449 (modified), to sign the initialed Form PTO-1449 (modified), and to return a copy of the same with the next communication to the Applicant(s).

Since copies of the cited references were previously submitted in prior U.S. Patent Application No. 09/801,151, copies of the cited references are not being submitted herewith. However, copies will be forwarded at the request of the Examiner.

In accordance with 37 CFR § 1.97(b), this information disclosure statement is being filed (i) within three months of the filing date of the above-identified patent application; (ii) within three months of the date upon which the above-identified patent application entered the national stage as set forth in 37 CFR § 1.491; or (iii) before the mailing date of a first Office Action on the merit for the above-identified patent application. Accordingly, no statement or fee is required.

Please charge any shortage in fees due in connection with the filing of this communication to Deposit Account No. 50-0206, and please credit any excess fees to such deposit account.

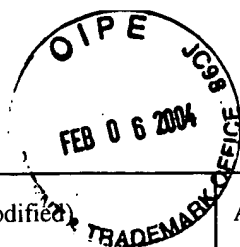
Respectfully submitted,

Hunton & Williams LLP

By: _____
Thomas E. Anderson
Registration No. 37,063

TEA/sdw

Hunton & Williams LLP
1900 K Street, N.W.
Washington, D.C. 20006-1109
Telephone: (202) 955-1500
Facsimile: (202) 778-2201

Date: February 6, 2004



PTO-1449 (Modified) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE INFORMATION DISCLOSURE STATEMENT BY APPLICANT	ATTY. DOCKET NO. 57941.000062	SERIAL NUMBER 10/716,595
	APPLICANT(S) MICHAEL FARMWALD ET AL.	
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	1.	4,330,852	May 18, 1982	Redwine et al.			
	2.	4,703,418	Oct. 27, 1987	James			
	3.	4,726,021	Feb. 16, 1988	Horiguchi et al.			
	4.	4,785,394	Nov. 15, 1988	Fischer			
	5.	4,870,562	Sept. 26, 1989	Kimoto et al.			

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	6.	S56-82961	July 7, 1981	Japan			YES
	7.	S57-14922	Jan. 26, 1982	Japan			YES
	8.	Sho 60-80193	May 8, 1983	Japan			YES
	9.	Sho 60-55459	Mar. 30, 1985	Japan			YES
	10.	S61-72350	April 14, 1986	Japan			YES
	11.	S63-142445	June 14, 1988	Japan			YES
	12.	B63-46864	Sept. 19, 1988	Japan			YES
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	22.	0 246 767	April 28, 1987	EPO			
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	25.	European Search Report for EPO Patent Application No. 00 101 1832
	26.	European Search Report for EPO Patent Application No. 89 30 2613
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	29.	H. Kuriyama et al., "A 4-Mbit CMOS SRAM WITH 8-NS SERIAL ACCESS TIME", IEEE Symposium On VLSI Circuits Digest Of Technical Papers, pp. 51-52, (June 1990)
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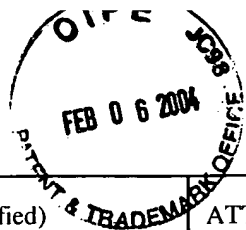


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	74.	5,301,278	04/05/94	Bowater et al.			
	75.	5,140,688	08/18/92	White et al.			
	76.	5,018,111	05/21/91	Madland			
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	79.	4,975,872	12/04/90	Zaiki			
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	89.	4,905,201	Feb. 27, 1990	Ohira et al.			
	90.	3,691,534	09/12/72	Veradi, et. al			
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	92.	4,536,795	08/20/85	Hirota, et. al			
	93.	4,629,909	12/16/86	Cameron			
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	96.	4,499,536	02/12/85	Gemma et al.			
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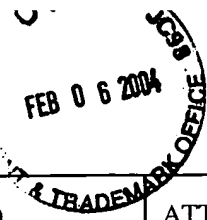
EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANSLATION YES/NO
	98.	EP 0424774	05/02/91	EPO			
	99.	EP 0449052	03/29/90	EPO			

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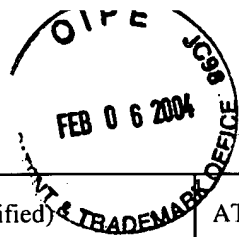
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	110.	EP 0218523	05/30/89	EPO			
	111.	JP-A-1- 236494	09/21/89	JP			YES
	112.	Sho 62-71428	03/27/87	JP			YES
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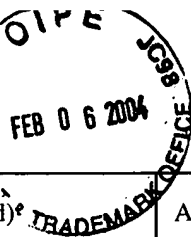
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	APPLICANT(S) MICHAEL FARMWALD ET AL.	
	FILING DATE November 20, 2003	GROUP ART UNIT Unassigned

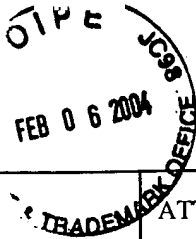
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	151.	4,763,249	08/09/88	Bomba et al.			
	152.	5,179,667	01/12/1993	Iyer			
	153.	5,029,124	07/02/1991	Leahy et al.			
	154.	4,878,166	10/31/1989	Johnson et al.			
	155.	4,851,990	07/25/1989	Johnson et al.			
	156.	4,839,801	06/13/1989	Nicely et al.			
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	158.	4,933,953	Jun. 12, 1990	Yagi			
	159.	5,133,064	Jul. 21, 1992	Hotta et al			
	160.	5,184,027	Feb. 2, 1993	Masuda et al.			
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	163.	SHO 58-192154	Nov. 9, 1983	Japan			NO
	164.	SHO 63-34795	Feb. 15, 1988	Japan			NO
	165.	SHO 61-107453	May 26, 1986	Japan			NO
	166.	SHO 63-91766	April 22, 1988	Japan			YES
	167.	SHO 62-16289	Jan. 24, 1987	Japan			NO
	168.	SHO 61-160556	Oct. 4, 1986	Japan			NO
	169.	JP 1284132	Nov 15, 1989	Japan			YES

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	170.	4,528,646	Jul. 9, 1985	Ochii et al.			
	171.	4,922,141	May 1, 1990	Lofgren et al.			
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	176.	EP 0 329 418 A2	Aug 23, 1989	EPO			
	177.	JP 1043894	Feb. 16, 1989	Japan			YES
	178.	sho 58-31637A	Feb 24, 1983	Japan			
	179.	sho 59-165285A	Mar. 11, 1983	Japan			
	180.	sho 60-261095A	June 6, 1984	Japan			
	181.	sho 63-300310	Dec. 7, 1988	Japan			
	182.	hei 2-8950	Jan 12, 1990	Japan			
	183.	sho 58-184626A	Oct 28, 1983	Japan			

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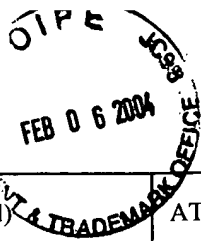
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	185.	5,157,776	Oct. 20, 1992	Foster			
	186.	5,023,838	Jun. 11, 1991	Herbert			
	187.	4,961,171	Oct. 2, 1990	Pinkham et al.			
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	207.	61028248	Feb. 7, 1986	Japan			

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	209.	"Intel MCS-4 Micro Computer Set", Intel Corporation, Santa Clara, CA, 1972, (pp.1-12)
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	214.	4,920,483	Apr. 24, 1990	Pogue et al.			
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	232.	0 126 976	Dec. 5, 1984	EPO			
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